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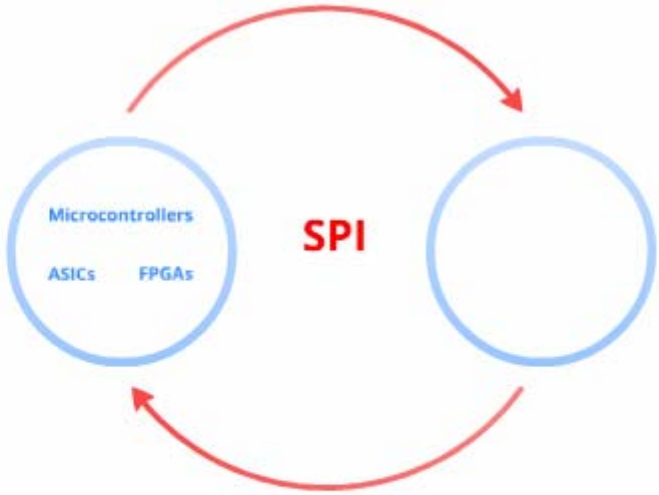
Serial Peripheral Interface

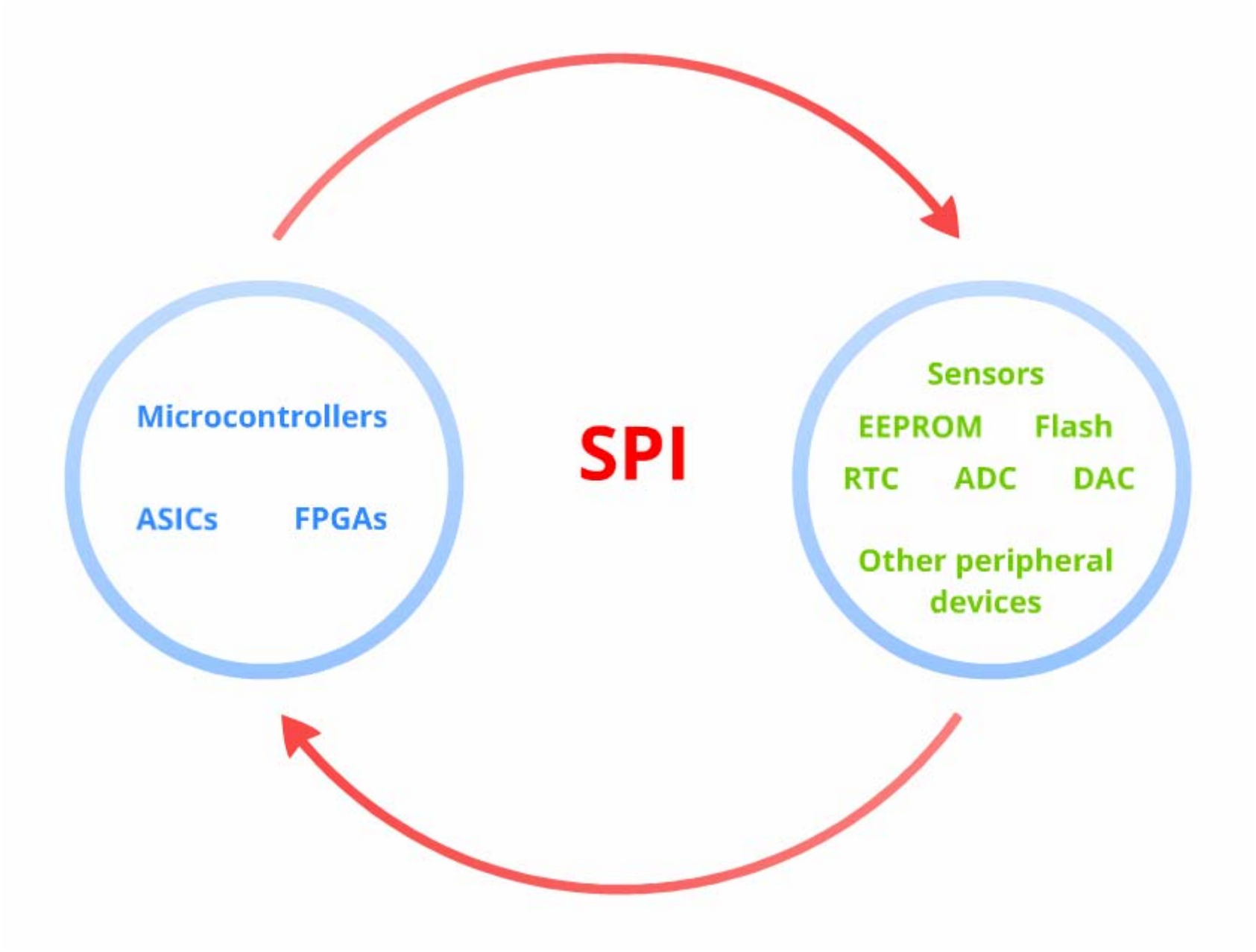
SPI

Serial Peripheral Interface

Motorola originally designed SPI for the MC68HCxx processors to communicate with peripheral devices.

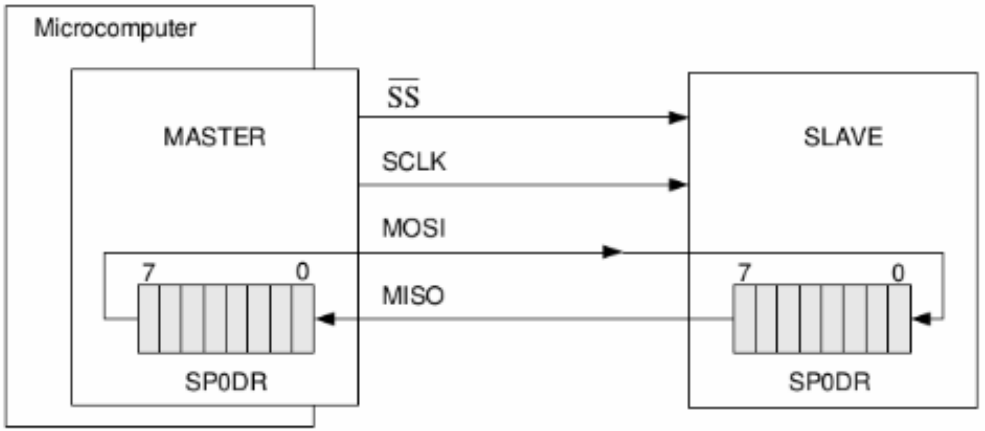
- ✔ Serial
- ✔ Synchronous
- ✔ Full Duplex




Microcontrollers
ASICs
FPGAs
SPI
Sensors
EEPROM
Flash
RTC
ADC
DAC
Other peripheral devices

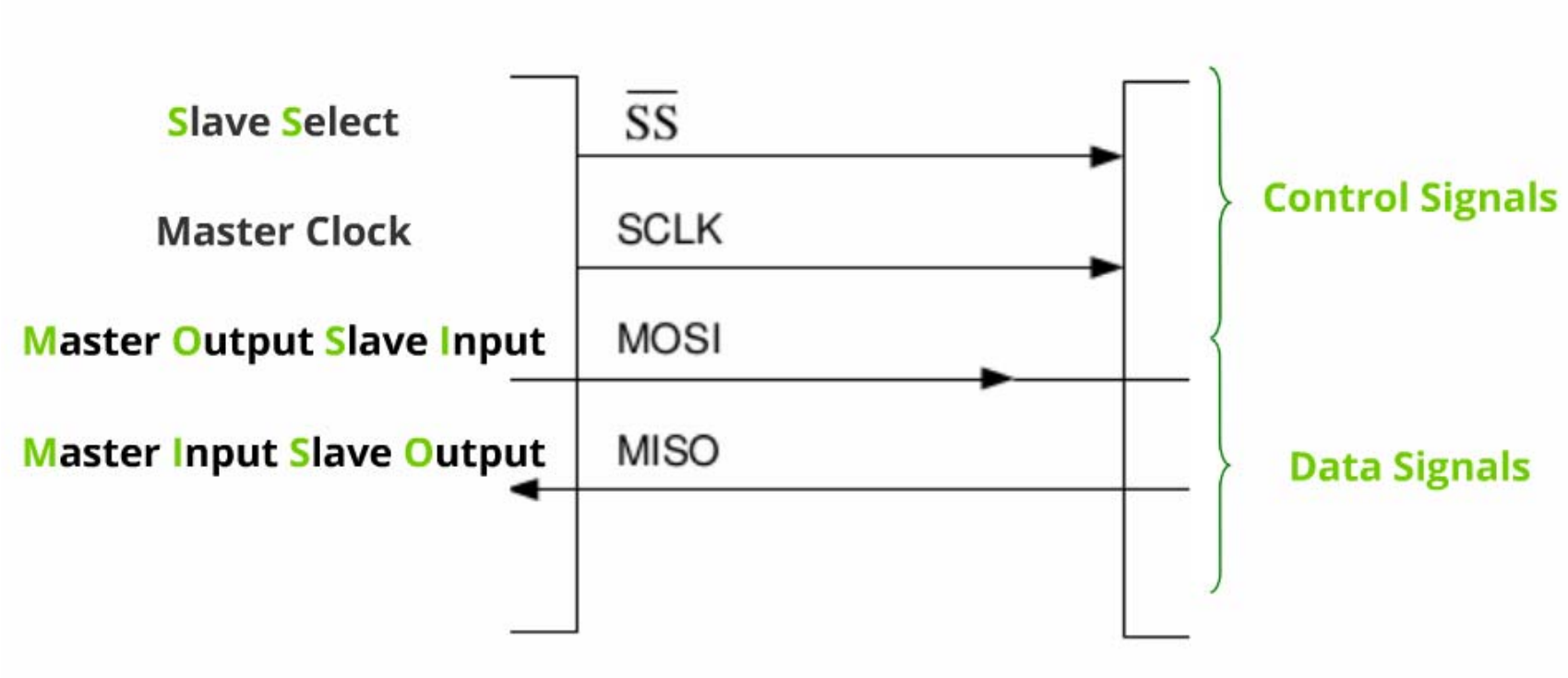
Serial Peripheral Interface

It is hard to find a formal separate 'specification' of the SPI bus – for a detailed 'official' description, one has to READ the microcontrollers data sheets and associated application notes.



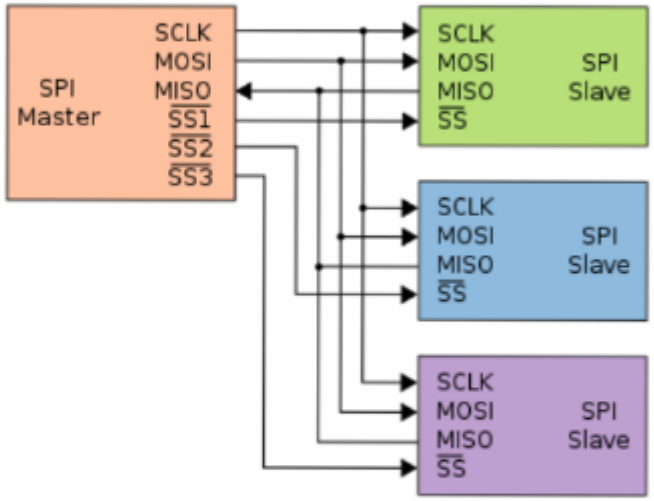
There is NO SPI protocol per se

- ✓ Transfer Size: 5-16 bits transfers
- ✓ Bandwidth: ~ 10 Mbps
- ✗ No acknowledgement mechanisms
- ✗ No flow control mechanisms
- ✗ No addressing


Slave Select
$\overline{SS}$
Master Clock
SCLK
Master Output Slave Input
MOSI
Master Input Slave Output
MISO
Control Signals
Data Signals

Serial Peripheral Interface

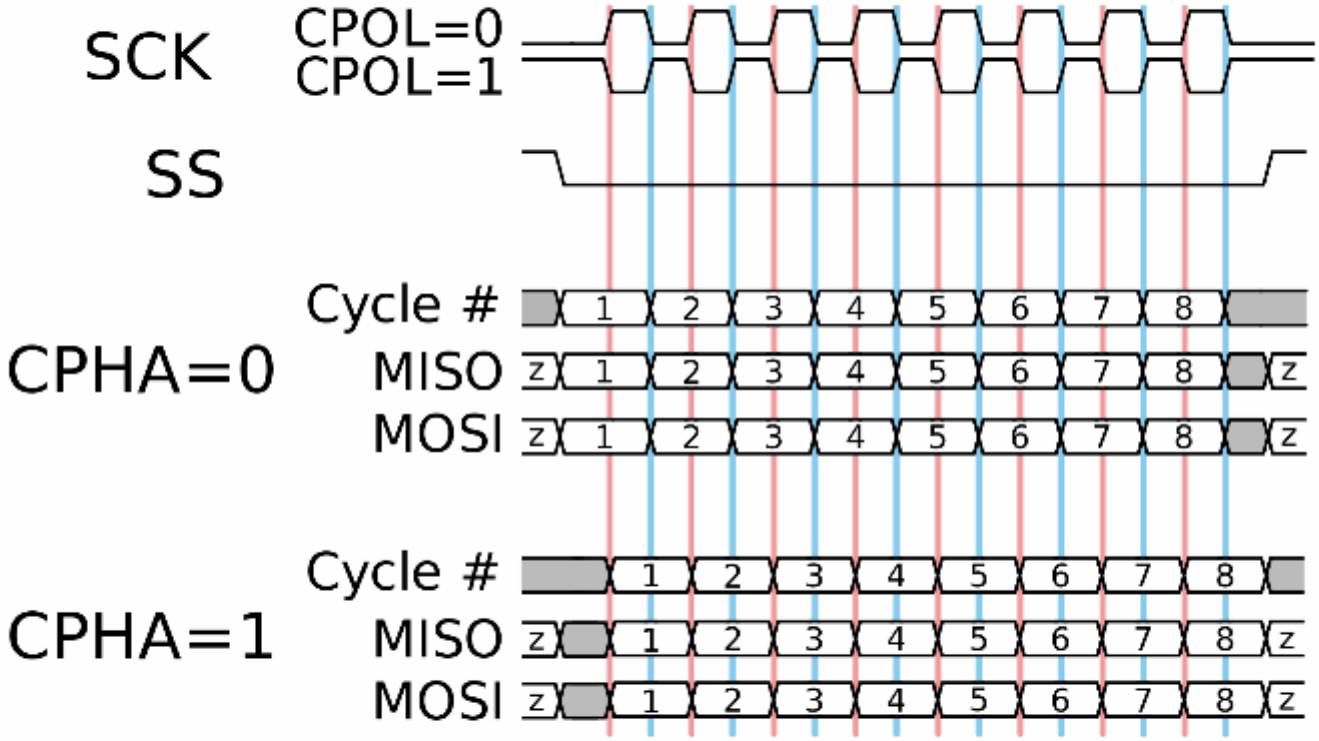
Multiple slaves



3 + N wire
N:= number of devices

Serial Peripheral Interface

Clock polarity and phase



Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

ADC TLV2553

TEXAS INSTRUMENTS

12-BIT, 200-KSPS, 11-CHANNEL, LOW-POWER, SERIAL ADC

FEATURES

- 12-Bit-Resolution A/D Converter
- Up to 200 KSPS (150 KSPS for 3 V) Throughput Over Operating Temperature Range With 12-Bit Output Mode
- 11 Analog Input Channels
- 3 Built-In Self-Test Modes
- Inherent Sample and Hold Function
- Linearity Error . . . ±1 LSB Max
- On-Chip Conversion Clock
- Unipolar or Bipolar Output Operation
- Programmable MSB or LSB First
- Programmable Power Down
- Programmable Output Data Length
- SPI Compatible Serial Interface With I/O Clock Frequencies up to 15 MHz (CPOL=0, CPHA=0)

In addition to the high-speed converter control ca… an on-cl… multi… of 1… or…

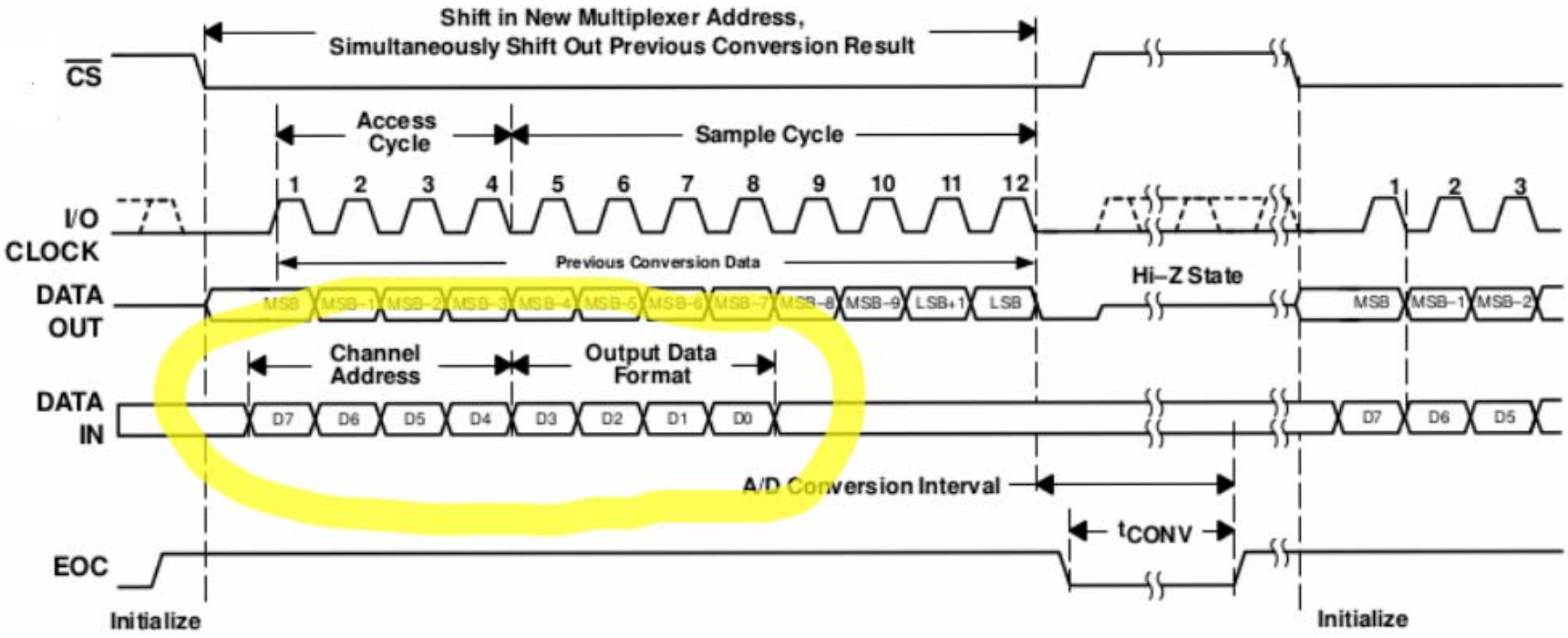
- ✔ Clock Frequency: 15 MHz
- ✔ Transfer Size: 12 Bits
- ✔ Clock Polarity: 0
- ✔ Clock Phase: 0

…perating…

The TLV2553I is characterized for o… T_A = –40°C to 85°C. See available op… package options.

DW AND PW PACKAGE
(TOP VIEW)

timing diagrams



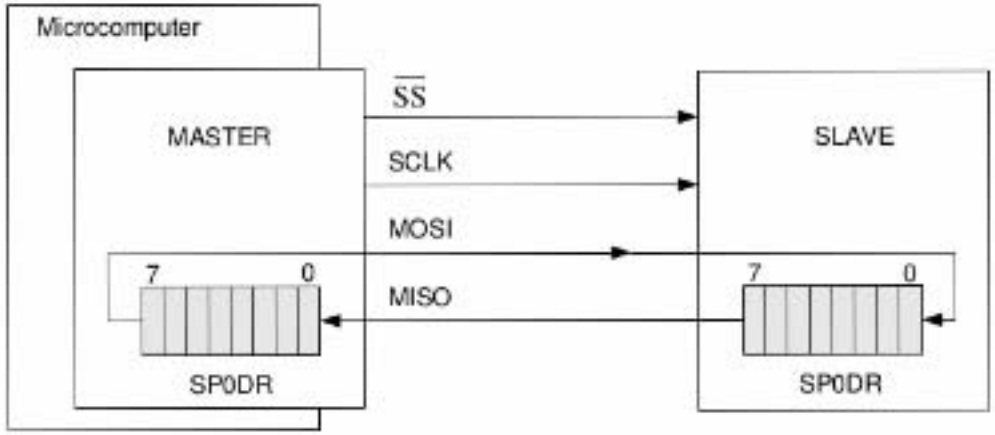
SDI D[7:4] Binary,	HEX	COMMAND
0000b	0h	SELECT analog input channel 0
0001b	1h	SELECT analog input channel 1
0010b	2h	SELECT analog input channel 2
0011b	3h	SELECT analog input channel 3
0100b	4h	SELECT analog input channel 4
0101b	5h	SELECT analog input channel 5
0110b	6h	SELECT analog input channel 6
0111b	7h	SELECT analog input channel 7
1000b	8h	SELECT analog input channel 8
1001b	9h	SELECT analog input channel 9
1010b	Ah	SELECT analog input channel 10
1011b	Bh	SELECT TEST, Voltage = (VREF+ + VREF–)/2
1100b	Ch	SELECT TEST, Voltage = REFM
1101b	Dh	SELECT TEST, Voltage = REFP
1110b	Eh	SW POWERDOWN (analog + reference)
1111b	Fh	Reserved

CFGR1

SDI D[3:0]	CONFIGURATION
D[3:2]	01: 8-bit output length X0: 12-bit output length (see Note) 11: 16-bit output length
D1	0: MSB out first 1: LSB out first
D0	0: Unipolar binary 1: Bipolar 2s complement

NOTE: Select 12-bit output mode to achieve 200 KSPS sampling rate.

Don't forget to check voltage levels between master and slaves!!!



Summary

Advantages

- Full Duplex
- High throughput
- Flexibility
- Simple hardware and firmware
- No patents issues

Disadvantages

- Does not scale well with multiple devices
- No acknoledgement, flow control or addressing mechanisms
- Supports only one master device